REMARKS

Claims 1-40 are currently pending with claims 8-14, 16-25, 31-33 and 36-40 being withdrawn from consideration. It is respectfully submitted that generic claim 1 is allowable and therefore these non-elected species claims should be rejoined and allowed with the application.

The Office Action includes a rejection of claims 1 and 3 under 35 U.S.C. § 102(b) as allegedly being anticipated by the Bowers et al. patent (U.S. Patent 5,985,687); a rejection of claims 2, 4-6, 26, 27 and 34 under 35 U.S.C. § 103, as allegedly being unpatentable over the Bowers et al. patent in view of he Nakamura patent (U.S. Patent 5,290,393); and a rejection of claims 7,15, 28-30 and 35 under 35 U.S.C. § 103 as allegedly being unpatentable over the Bowers et al. patent in view of the Nakamura patent and in further view of the Chen et al. patent (U.S. Patent 5,927,995). These rejections are respectfully traversed.

The Bowers et al. patent is primarily directed to a method of making cleaved facets for laser fabrication. It discloses depositing a GaN buffer layer, a GaN device layer and an InN fusion layer on a sapphire substrate and then thermally fusing that stacked structure onto a GaAs or InP substrate. In Figures 4a and 4b, a sacrificial ZnO layer 24 is deposited on the sapphire substrate and acts as a sacrificial layer to remove the sapphire substrate.

Applicants respectfully submit that the Bowers patent does not anticipate nor render obvious any of the claims.

Original claim 1 recited a compound semiconductor substrate fabrication method comprising preparing a base substrate, forming a first buffer layer on the prepared base

substrate, forming a semiconductor layer on the first buffer layer and removing the base substrate. It is emphasized that the preamble identified this as a semiconductor substrate fabrication method. This is because the resulting product is a substrate the formed semiconductor layer acting as the resulting substrate. The substrate can be a GaN substrate which does not undergo cracking due to thermal stresses as explained in the background section of the present application.

What is lacking in Bowers et al. patent is the idea that a substrate is being fabricated. Both the sapphire substrate and the GaAs or InP substrate are preformed and simply thermally fused together. Neither involves forming a semiconductor layer on a first buffer layer such that the semiconductor layer is the substrate resulting from the fabrication method upon removal of the base substrate.

Additionally, third and fourth steps in the amended claim 1 of the present application, i.e., forming a semiconductor layer on the first buffer and removing the base substrate such that said semiconductor layer is a substrate, are consecutively performed. That is, processes like a process of fusing a GaAs of InP substrate 10 and a second multiple layered structure 12 described in the Bowers et al. patent cited by the Examiner are not added between the third step and the fourth step of the present application. In the Bowers et al. patent, a process of removing a portion or all of a sapphire substrate 14 can not be performed without the processes of forming a fusion layer 20 on a GaN device layer 18 and respectively fusing a GaAs or InP substrate 10 and a second multiple layered structure 12. Therefore, it is inappropriate to assert that removing the base substrate as presented in the present application is disclosed in the Bowers et al. patent.

Hence, Applicants respectfully submit that the Bowers et al. patent does not anticipate claims 1 or 3, and insofar as the remainder of the rejections are based on the Bowers et al. patent, Applicants respectfully submit that all claims are allowable. For completeness, however, the secondary references will be briefly discussed.

The Nakamura patent is directed to a crystal growth method and is cited for allegedly teaching the forming of a second buffer layer on the semiconductor layer before removing the base substrate. First, it is noted that the Nakamura patent does not cure the deficiencies of the Bowers et al. patent identified above. Second, it is not clear why the Office assumes that the formation of a second buffer layer in the Bowers et al. system would be advantageous. The Nakamura patent identifies the advantages of a second buffer layer placed between a p-type and a n-type GaN layer. This structure is not in the Bowers et al. patent and hence it is not clear why one would choose to modify the Bowers et al. structure when it does not have the pattern of an n-type GaN layer, a buffer layer and a p-type GaN layer as shown in the top section of Figure 12. Regardless of whether there is motivation for modification, it is noted that the hypothetical combination would still not result in the present invention for the reasons explained above.

With respect to the Chen et al. patent, it is noted that it is directed to the reduction of threading dislocations and cited by the Office for allegedly teaching that he first and second buffer layers can be formed of multi-semiconductor layers. Even if this is true, it would still not result in the present invention insofar as none of the patents identifies the recitations of claim 1, as articulated above. Hence, even if the hypothetical combination were suggested by the prior art, it would still not result in the present invention.

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above-captioned application. Should any residual issues exist, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

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